CLAIMS

1. A method for measuring a parameter selected from the group consisting of voltage, temperature, and integrated circuit process conditions, the method comprising:

providing a primary delay line and a timer delay line;

applying an input voltage to said primary delay line;

applying a reference voltage to said timer delay line;

propagating a delay signal through said primary delay line;

propagating a timer signal through said timer delay line;

establishing a first sampling period based on said timer signal propagation;

measuring a first extent of delay signal propagation along said primary delay line during said first established sampling period; and

using said delay signal propagation first extent to provide an output signal characteristic of one or more of said parameters.

2. The method of claim 1 wherein said propagating said delay signal comprises cycling said delay signal through said primary delay line a plurality of times.

3. The method of claim 1 wherein said propagating said timer signal comprises cycling said timer signal through said timer delay line a plurality of times.

4. The method of claim 1 wherein said using comprises finding the difference between a timer delay extent of propagation through said timer delay line and a corresponding primary delay first extent of propagation through said primary delay line to determine a difference code.

5. The method of claim 4 wherein said providing a primary delay line and a timer delay line comprises providing a primary delay ring and a timer delay ring, and said finding the difference comprises counting a predetermined number of cycles of said timer signal through said timer delay ring and counting the number of cycles of said delay signal through said primary delay ring while said timer signal cycles through said predetermined number of cycles.

6. The method of claim 5 wherein said using further comprises gain calibration.

7. The method of claim 6 wherein said using further comprises mismatch

correction.

8. The method of claim 5 wherein said using further comprises mismatch correction.

9. The method of claim 1 wherein said using further comprises gain calibration.

10. The method of claim 6 wherein said gain calibration comprises defining a calibration period and measuring a calibration extent of propagation of said timer signal through said timer delay line during said calibration period.

11. The method of claim 1 wherein said using further comprises mismatch correction.

12. The method of claim 12 wherein said mismatch correction comprises:

applying said reference voltage to said primary delay line;

establishing a mismatch sampling period based on said timer signal propagation through said timer line;

measuring a mismatch extent of delay signal propagation along said primary delay line during said mismatch sampling period; and

finding the difference between said mismatch extent of delay and said first extent of delay to determine a mismatch-corrected difference code.

13. The method of claim 1 wherein said establishing comprises starting said first sampling period when said timer signal begins propagating through said timer delay line and ending said first sampling period when said timer signal reaches a specific point along said timer delay line.

14. The method of claim 1 wherein said measuring comprises detecting output logic states of delay cells in said primary delay line.

15. The method of claim 14 wherein said using comprises converting said output logic states into digital code.

16. The method of claim 14 wherein said using comprises converting said output logic states into thermometer code.

17. The method of claim 1 wherein said providing a primary delay line comprises providing a plurality of primary delay line delay cells.

18. The method of claim 17 wherein said providing a timer delay line comprises providing a plurality of timer delay line delay cells.

19. The method of claim 1 wherein said providing comprises incorporating said primary delay line and said timer delay line into a single integrated circuit.

20. The method of claim 19 wherein said providing comprises forming said primary delay line and said timer delay line sufficiently close to one another in said integrated circuit so that they are substantially always at the same temperature.

21. The method of claim 1 wherein said providing comprises forming said timer delay line and said primary delay line with the same process conditions.

22. The method of claim 1 wherein said parameter consists essentially of voltage.

23. The method of claim 1 wherein said parameter consists essentially of temperature.

24. The method of claim 1 wherein said parameter consists essentially of integrated circuit process conditions.

25. An analog-to-digital converter (ADC) comprising:

a source of an input voltage;

a source of a reference voltage;

a primary delay line connected to said source of an input voltage, and having a delay signal input and a plurality of tap outputs;

a timer delay line connected to said source of a reference voltage and having a timer signal input and a timer signal output;

a delay signal source connected to said delay signal input and said timer delay signal input, and

a digital output circuit coupled to said tap outputs and said timer signal output to provide a digital output indicative of a difference between said input voltage and said reference voltage.

26. The ADC of claim 25 wherein said ADC is implemented entirely with digital logic gates.

27. The ADC of claim 25 wherein said ADC includes no analog components.

28. The ADC of claim 25 wherein said primary delay line and said timer delay line are incorporated into a single integrated circuit.

29. The ADC of claim 25 wherein said primary delay line comprises a plurality of delay cells.

30. The ADC of claim 29 wherein each of said delay cells comprises a digital logic element.

31. The ADC of claim 25 wherein said timer delay line is substantially one-half the length of said primary delay line.

32. The ADC of claim 25 wherein said delay signal source simultaneously provides a delay signal to said delay signal input and a timer signal to said timer signal input.

33. The ADC of claim 32 wherein said delay signal and said timer signal as provided by said delay signal source are the same signal.

34. The ADC of claim 25 wherein said digital output circuit comprises an array of flip-flop circuits.

35. The ADC of claim 25 wherein said digital output circuit includes a counter.

36. The ADC of claim 25 wherein said digital output circuit includes a shift register.

37. The ADC of claim 25 wherein said primary delay line is a flat delay line.

38. The ADC of claim 25 wherein said primary delay line is a folded delay line.

39. The ADC of claim 25 wherein said primary delay line comprises a number of delay cells corresponding to the desired least significant bit (LSB) voltage step-size.

40. The ADC of claim 25 wherein said primary delay line comprises a number of delay cells smaller than the number of cells required to produce the desired least significant bit (LSB) voltage step-size.

41. The ADC of claim 25 wherein said timer delay line is a flat delay line.

42. The ADC of claim 25 wherein said timer delay line is a folded delay line.

43. The ADC of claim 25 wherein said digital output circuit includes a gain calibration circuit.

44. The ADC of claim 25 wherein said digital output circuit includes a mismatch correction circuit.

45. A method for converting an analog voltage to a digital signal, the method comprising:

applying an analog input voltage to delay cells in a primary delay line;

propagating a delay signal through said primary delay line;

adjusting a sampling period for said delay signal propagation based on factors affecting a speed of said delay signal propagation other than said analog input voltage;

measuring an extent of delay signal propagation during said adjusted sampling period; and

responsive to said measured extent of propagation, providing a digital output signal indicative of a magnitude of said analog voltage.

46. The method of claim 45 wherein said adjusting comprises adjusting said sampling period for temperature variation in said primary delay line.

47. The method of claim 45 wherein said adjusting comprises adjusting said sampling period in response to process conditions in said primary delay line.

48. The method of claim 45 wherein said adjusting comprises:

providing a timer delay line having delay cells powered by a reference voltage;

propagating a timer signal through said timer delay line; and

establishing said sampling period based on a duration of said timer signal propagation through said timer delay line.

49. The method of claim 45 wherein said measuring comprises determining output logic states of said delay cells at an end of said adjusted sampling period.

50. The method of claim 45 wherein said providing comprises expressing said digital output signal in digital code.

51. The method of claim 45 further comprising expressing said digital output signal in thermometer code.